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RONALD P KANANEN ESQ
RADER FISHMAN AND GRAUER
THE LION BUILDING
1233 20TH STREET N W SUITE 501
WASHINGTON, DC 20036

EXAMINER
PADMANABHAN, MANO

ART UNIT	PAPER NUMBER
2671	

DATE MAILED: 02/28/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/283,231	KUROSE, YOSHIKAZU	
	Examiner	Art Unit	
	Mano Padmanabhan	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *17 October 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *17 October 2001* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Status of claims

Claims 1-40 are in the Application.

Claims 1-40 are rejected.

Response to Amendment

Applicants response and amendments of 10/17/2001 to the office action mailed on 7/31/2001 have been fully considered, but they are not persuasive. The 103 rejections from the last office action are maintained, and are re-stated below.

Claim Objections

The amendments have overcome the claim objections.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 5-8, 10, 22-24, and 26-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dawson (US Patent 5,179,638), in view of Kiyoto (09130570: Patent Abstracts of Japan: Publication Date 16-05-97).

Claim 27, claims a method of expressing an image as a composite of graphic units of predetermined shape, comprising the steps of judging whether or not a pixel is positioned within a unit graphic for each of the pixels among a plurality of pixels being simultaneously processed in parallel in plurality of pixel processing circuits, stopping the operation of pixel processing for pixels not within the graphic units based on the outcome of the judging step.

As per claim 27, Dawson teaches distributed processing using parallel pipelines (processing a plurality of pixels in a plurality of pixel processing circuits), and then recombining the parallel pixel flow into a single memory module known as a frame buffer (Col.2: lines 46-50; Col.11: lines 51-62). Dawson also teaches interpolating values for the interior points (Col.6: lines 65-66), thus teaching implicitly, a judging means that determined these pixels to be interior pixels. Dawson, while not teaching setting a valid bit flag for this condition, does teach setting a polygon "end" bit in the last vertex of the polygon, and checking that flag while rendering the primitive (setting a bit to flag a condition). Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to set a valid bit when the pixels were judged to be inside the polygon, and check the flag during pixel value computations, in order to reduce computational overhead. Dawson however fails to teach stopping the operation of the pixel processing circuits for pixels that do not lie within the unit graphics. Kiyoto teaches a method to prevent useless power consumption by stopping the application of an image clock signal to a processing block not in use (Abstract). Hence it would have been obvious to one of ordinary skill in the art at the time the invention was made, to use Kiyoto's teaching to stop the

operation of the pixel processing circuits for pixels that do not lie within the unit graphics in the invention of Dawson, in order to prevent useless power consumption.

Claim 22 is similar to claim 27, and hence is rejected with the same rationale.

Claim 28 adds to claim 27, the steps of supplying clock signal to pixel processing circuits for pixels within the graphic unit, and stopping the supply of clock signal to circuits for pixels that do not lie inside the graphic unit.

As per claim 28, Kiyoto teaches a supply/inhibit signal generating section, generating a signal to inhibit the application of the image clock signal to a processing block not relating to the image processing (Abstract).

Claim 23 is similar to claim 28, and hence is rejected with the same rationale.

Claim 29 adds to claim 28, the step of each of the pixel processing circuits performing pipeline processing by a plurality of processing circuits connected in series.

As per claim 29, Dawson teaches a plurality of processing circuits connected in series, for example, symbol generator, geometry engine, tiling engine, etc. (Fig.5).

Claim 24 is similar to claim 29, and hence is rejected with the same rationale.

Claim 26 adds to claim 22, the step of processing the R, G, B output values of a pixel.

As per claim 26, Dawson teaches that the R, G, B values are independently calculated when rendering polygons (Col.8: lines 55-58).

Claims 1-3 and 5-8 are claims to apparatus that perform the methods of claims 22-24 and 26-29 respectively, and hence, are rejected with the same rationale.

Claim 10 adds to claim 6 the steps of the pixel position judging circuit adding validity data to of the result of the judgement to pixel data, and the control circuit judging whether to stop the operation of the pixel processing circuits based on the validity data.

As per claim 10, Dawson teaches interpolating values for the interior points (Col.6: lines 65-66), thus teaching implicitly a judging means that determined these pixels to be interior pixels. Dawson does not teach setting a valid bit flag for this condition. However, Dawson teaches setting a polygon "end" bit in the last vertex of the polygon, and checking that flag while rendering the primitive. Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to set a valid flag when the pixels tested were judged to be inside the polygon, and check the flag during pixel value computations, so that wastage of resources, in determining values for pixels that will not be displayed, may be avoided.

4. Claims 4, 9, 25, and, 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dawson (US Patent 5,179,638), in view of Kiyoto (09130570: Patent Abstracts of Japan: Publication Date 16-05-97), as applied to claim 27, and further in view of Duluk, Jr. (US Patent 5,977,987).

Claim 30 adds to claim 29, the step of the pixel processing circuit having a flag storage portion, connected in series to constitute a shift register, and the shift register being used to control the pipeline processing and supply of clock signal.

As per claim 30, Duluk teaches a rendering system wherein a flag memory storage means is used to store a flag bit equal to the query result, and a shifting means for conditionally shifting data stored in data fields, wherein the shifting means includes a shift register bit connected to the storage bits of storage means (Claims 29 and 34). Hence it would have been obvious to one of ordinary skill in the art at the time the invention was made, to connect the flag storage portion to the shift register in series as taught be Duluk, in the invention of Dawson, to control the pipeline processing, since use of registers in processing was known to be much faster than access to other memory locations, since the registers resided in the CPU.

Claim 25 is similar to claim 30 and hence is rejected with the same rationale.

Claims 4 and 9 are claims to apparatus that perform the methods of claims 25 and 30 respectively, and hence, are rejected with the same rationale.

5. Claims 11-13, 15, 16-19, 21, 31-33, 35-38, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dawson (US Patent 5,179,638), in view of Huxley (US Patent 5,742,796), and Kiyoto (09130570: Patent Abstracts of Japan: Publication Date 16-05-97).

Claim 31 claims a image processing method comprising the steps of using a plurality of pixel processing circuits to simultaneously blend a plurality of first pixel data and a plurality of second pixel data indicated by a blending ratio data set for each pixel, judging based on the blending ratio data whether to perform said blending by pixel processing circuits, and stopping the operation of the corresponding pixel circuits when judging that they will not perform said blending.

As per claim 31, Dawson teaches distributed processing using parallel pipelines (processing a plurality of pixels in a plurality of pixel processing circuits), and then recombining the parallel pixel flow into a single memory module known as a frame buffer (Col.2: lines 46-50; Col.11: lines 51-62). Dawson however fails to teach the use of blending ratio data in pixel processing. Huxley teaches an alpha blend unit (Col.61), which blends the source color and destination color in the given ratios, to produce an output color, as shown by the equation (Col.61: line 16). Huxley also teaches a NoAlphaBuffer bit in the AlphaBlendMode message that controls alpha blending, wherein the setting of the NoAlphaBuffer bit or the absence of an alpha value causes the alpha blending to be bypassed. Hence it would have been obvious to one of ordinary skill in the art at the time the invention was made, to include the blending ratio pixel processing of Huxley in the texture engine of Dawson, in order to provide more realistic results. Dawson and Huxley, however fails to teach stopping the operation of the pixel processing circuits for pixels that do not lie within the unit graphics. Kiyoto teaches a method to prevent useless power consumption by stopping the application of an image clock signal to a processing block not in use (Abstract). Hence, it would have been obvious to one of ordinary skill in the art

at the time the invention was made, to use Kiyoto's teaching to stop the operation of the pixel processing circuits for pixels that do not lie within the unit graphics or do not need alpha blending, in the invention of Dawson and Huxley, in order to prevent useless power consumption.

Claims 32-33 are similar to claims 28 and 29 respectively, and hence are rejected with the same rationale.

Claim 35 claims a method of expressing an image as a composite of graphic units of predetermined shape, comprising the steps of using a plurality of pixel processing circuits to blend a plurality of first pixel data and a plurality of second pixel data indicated by a blending ratio data set for each pixel, judging whether or not a pixel is positioned within a unit graphic for each of the pixels among a plurality of pixels being simultaneously processed in parallel in plurality of pixel processing circuits, stopping the operation of pixel processing for pixels not within the graphic units based on the outcome of the judging step.

As per claim 35, Dawson teaches distributed processing using parallel pipelines (processing a plurality of pixels in a plurality of pixel processing circuits), and then recombining the parallel pixel flow into a single memory module known as a frame buffer (Col.2: lines 46-50; Col.11: lines 51-62). Dawson also teaches interpolating values for the interior points (Col.6: lines 65-66), thus teaching implicitly, a judging means that determined these pixels to be interior pixels. Dawson fails to teach blending of pixel data. Huxley teaches an alpha blend unit (Col.61), which blends the source color (first pixel data) and destination color (second pixel data)

in the given ratios, to produce an output color (third pixel data), as shown by the equation (Col.61: line 16). Huxley also teaches a NoAlphaBuffer bit in the AlphaBlendMode message that controls alpha blending, wherein the setting of the NoAlphaBuffer bit or the absence of an alpha value causes the alpha blending to be bypassed. Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to combine the blending ratio pixel processing of Huxley with the interpolation processing of Dawson, to interpolate the color texture values for the interior pixels, for greater efficiency in pixel processing. Dawson and Huxley, however fails to teach stopping the operation of the pixel processing circuits for pixels that do not lie within the unit graphics. Kiyoto teaches a method to prevent useless power consumption by stopping the application of an image clock signal to a processing block not in use (Abstract). Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to use Kiyoto's teaching to stop the operation of the pixel processing circuits for pixels that do not lie within the unit graphics or do not need alpha blending, in the invention of Dawson and Huxley, in order to prevent useless power consumption.

Claim 36 claims a image processing method comprising the steps of using a plurality of pixel processing circuits to process simultaneously, to produce a plurality of second pixel data from a plurality of first pixel data, comparing depths of plurality of first pixel with the depths of plurality of third pixels stored in a storage unit, judging whether or not to rewrite the third pixel data by the second pixel data, and stopping the operation of the corresponding pixel circuits when judging that they will not perform said rewrite.

As per claim 36, Dawson teaches distributed processing using parallel pipelines (processing a plurality of pixels in a plurality of pixel processing circuits), and then recombining the parallel pixel flow into a single memory module known as a frame buffer (Col.2: lines 46-50; Col.11: lines 51-62), thus also teaching producing plurality of second pixel data from a plurality of first pixel data. Dawson however does not teach depth comparison between pixel data. Huxley also teaches a depth test, which compares a new fragment's depth (second depth data of third pixel data), against the corresponding depth in the depth buffer (first depth data of first pixel data), and updating the frame buffer if the test passed, and ignoring the new fragment depth data if the test failed (Col.7: lines 8-33, Col.10: lines 8-60, Col.31: lines 12-20, Col.51: lines 25-65). Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to use the depth test as taught by Huxley, in the texture engine of Dawson, in order to be able to render the images in the correct perspective, taking into account the occluding properties of the objects rendered. Dawson and Huxley, however fails to teach stopping the operation of the pixel processing circuits for pixels that do not lie within the unit graphics. Kiyoto teaches a method to prevent useless power consumption by stopping the application of an image clock signal to a processing block not in use (Abstract). Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to use Kiyoto's teaching to stop the operation of the pixel processing circuits for pixels that do not lie within the unit graphics or do not need alpha blending, in the invention of Dawson and Huxley, in order to prevent useless power consumption.

Claims 37 and 38 are similar to claims 28 and 29 respectively, and hence are rejected with the same rationale.

Claim 40 claims a image processing method comprising the steps of using a plurality of pixel processing circuits to process simultaneously, to produce a plurality of second pixel data from a plurality of first pixel data, comparing depths of plurality of first pixel with the depths of plurality of third pixels stored in a storage unit, judging whether or not to rewrite the third pixel data by the second pixel data, and judging whether or not a pixel is positioned within a unit graphic for each of the pixels among a plurality of pixels being simultaneously processed in parallel in plurality of pixel processing circuits, and stopping the operation of the corresponding pixel circuits when judging that they will not perform said rewrite, or the pixel is not positioned within the unit graphic.

Claim 40 is a combination of claims 35 and 36, and hence is rejected with the same rationale as claims 35 and 36.

Claims 11-13 are claims to apparatus that perform the methods of claims 31 and 33 respectively, and hence, are rejected with the same rationale.

Claim 15 adds to claim 11 the steps of providing a storage circuit for storing second pixel data, and the control circuit rewriting the second pixel data by the first pixel data when blending will not be performed, and rewriting by the third pixel data when blending will be performed.

As per claim 15, Huxley teaches an alpha blend unit (Col.61), which blends the source color (first pixel data) and destination color (second pixel data) in the given ratios, to produce an output color (third pixel data), as shown by the equation (Col.61: line 16). Huxley also teaches a NoAlphaBuffer bit in the AlphaBlendMode message that controls alpha blending, wherein the setting of the NoAlphaBuffer bit or the absence of an alpha value causes the alpha blending to be bypassed, and when the alpha blending is disabled, the color is passed on unchanged. It is obvious from the equation $C_o = C_sS + C_dD$, that when there is no blending, the source color is the output color, implying that the second pixel data is replaced by the first pixel data when blending will not be performed, and, the output color (third pixel data) is written to the destination buffer (second pixel data), otherwise. Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to include the alpha blending unit in the texture engine of Dawson, in order to render objects in proper perspective.

Claims 16-19 are claims to apparatus that perform the methods of claims 35-38 respectively, and hence, are rejected with the same rationale.

Claim 21 is a claim to an apparatus that performs the method of claim 40, and hence, is rejected with the same rationale.

6. Claims 14, 20, 34, and, 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dawson (US Patent 5,179,638), in view of Huxley (US Patent 5,742,796), and Kiyoto

(09130570: Patent Abstracts of Japan: Publication Date 16-05-97), as applied to claims 11, 17, 31, and 36 respectively, and further in view of Duluk, Jr. (US Patent 5,977,987).

As per claims 14, 20, 34, and 39, Duluk teaches a rendering system wherein a flag memory storage means is used to store a flag bit equal to the query result, and a shifting means for conditionally shifting data stored in data fields, wherein the shifting means includes a shift register bit connected to the storage bits of storage means (Claims 29 and 34). Hence it would have been obvious to one of ordinary skill in the art at the time the invention was made, to connect the flag storage portion to the shift register in series as taught be Duluk, in the invention of Dawson, to control the pipeline processing, since use of registers in processing was known to be much faster than access to other memory locations, since the registers resided in the CPU.

Response to Arguments

1. Applicant's arguments filed 10/17/2001 have been fully considered but they are not persuasive.

2. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., only processing pixels that lie inside the polygon) are not recited in the rejected claim(s). It is also noted that the order of the steps is not enumerated in the claims. Dawson teaches recombining parallel pixel flow, thus teaching parallel pixel processing circuits, and also differentiates between interior and external points, and also teaches setting a bit to flag a condition. Kiyoto

teaches applying optional image processing to the image data, and use of clock signals to processing blocks (devices) not in use. Since pixel processing circuits are devices, similar to the processing blocks, it would have been obvious to one of ordinary skill in the art at the time of the invention to apply a similar mechanism to inhibit the pixel processors. As per the argument that Kiyoto does not teach a device for use with "polygon rendering", it is noted that Kiyoto does deal with image processing devices, and image processing means wherein pixel data is generated from image data input.

3. As per the argument that Huxley does not teach a judging step that controls whether or not the pixel processing circuits will perform blending, it is noted that Huxley teaches the use of NoAlphabuffer bit in the AlphaBlendMode message that is received by the pixel processing circuits, thus teaching a judging means that determines whether Alpha blending will be performed based on the presence/absence of alpha values for the pixel, and Kiyoto makes it obvious to stop the pixel processing circuits that do not have data to be processed. As per the argument regarding claims 12 and 32 that Huxley teaches away from stopping a pixel processing circuit for alpha blending by stating that the messages should continue to be passed to other units, it is noted that the pixel processing circuits would still need to process other attributes associated with the pixel in subsequent clock cycles, and hence, Huxley is not seen to teach away from what is claimed. As per the arguments regarding claims 17 and 36 regarding Huxley, the applicant is referred to the remarks above regarding claims 12 and 32.

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mano Padmanabhan whose telephone number is 703 306-2903. The examiner can normally be reached on Mon-Thurs: 7-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Zimmerman, can be reached at 703 305-9798.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Mano Padmanabhan

February 22, 2002

MARK ZIMMERMAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600